Remarks

Claims 1-7, 9-32, and 37-39 are pending in the present application. By this amendment, claims 1, 10, 27 and 37 have been amended. Thus, claims 1-7, 9-32, and 37-39 remain.

Applicant notes that the docket number for the present application is MIPS.0139-00-US (not MIPS.0140-00-US). Applicant would appreciate the examiner changing the attorney's docket number, if possible.

Claim Rejections under 35 USC §112

The examiner rejected claims 1-9 under 35 USC 112, second paragraph, as being indefinite because in the Examiner's opinion, it is unclear as to whether the interrupt register is part of the status register, or whether it is separate from the status register. Although applicant believes that the claim as originally submitted was clear, applicant has amended claim 1 to clarify that the interrupt register and vector table are part of the status register. However, the Examiner will appreciate that the term status register, as referenced in the claim, means the vector table and interrupt register. That is, no other limitation to the term "status register" should be given other than what is directly within the body of the claim, as amended. In view of the foregoing amendment, applicant respectfully requests the examiner to withdraw his rejection of these claims.

Claim Rejections under 35 USC §103

The examiner rejected claims 1, 2, 4, 5, 6, 7, 9, 10, 13, 14, 17, 22, 23, 24, 27, 29 and 30 under 35 USC 103(a) as being unpatentable over US Patent Number 5,371,872 to Larsen et al. ("Larsen") and US Patent Number 6,499,078 to Beckert et al. ("Beckert"). Applicant respectfully traverses.

Before a claim by claim analysis is provided, a brief overview of the art cited by the examiner is considered helpful.

With respect to Larsen, this patent is directed to an interrupt controller, in conjunction with a cache memory controller, which can be set to prevent or allow use of the cache for different interrupts. Referring to Figure 2 of Larsen, an interrupt controller 28 is provided, along with a cache controller 30. The interrupt controller 28 has external interrupt signals 28, and internal interrupt signals 26. The examiner points this out when

he references Larsen, Col. 5, lines 57-60 and 60-63. In addition, the interrupt controller 28 is coupled to a program status vector register 32. Applicant understands the program status register 32 to provide status information 36, relating to interrupts, for information in the cache. The status information is particularly shown in Figure 3. The status information lets the interrupt controller 28 know, for a particular interrupt, whether information related to the interrupt can be fetched from main memory, or the cache, whether the information can be locked or not locked in the cache, and whether data related to the interrupt can be placed in the cache. It appears from Larsen (see Col. 6, lines 28-31) that for each particular interrupt level [which applicant presumes is predefined], a series of program status words 34a-34n are stored to provide program status for a particular interrupt level. Thus, a first interrupt level would have a first program status word 34a, a second interrupt level would have a second program status word 34b, etc., where each program status word would indicate whether an interrupt at that level could use the cache, and to what extent it could use the cache. This is explained at Col. 7, lines 34-38. Thus, Larsen is interested in taking pre-existing interrupt levels, and coupling them to a cache controller so that the user can define how each interrupt level can use the cache.

In contrast, applicant's invention is not associating pre-existing interrupt levels with cache use. Rather, applicant's invention is directed at allowing a programmer to specify new interrupt levels within a pre-existing architecture, and define target vectors for these interrupt levels, to allow modifiable interrupt handling, including the time required to service an interrupt, for the new intermediate interrupts.

With respect to Beckert, this patent is directed to an interrupt handler which is external to a microprocessor. The interrupt handler has a programmable prioritized interrupt array with programmable registers that identify priority levels (see Abstract). The interrupt handler has a prioritized interrupt array 40 partitioned into a mask register 44 and a priority/address register 46. The priority/address register 46 has a priority field 48 that holds a priority level of an associated interrupt. See Col. 4, lines 3-32. Thus, all interrupts handled by the interrupt handler, have a priority field for which a programmed priority is assigned.

In contrast, applicant's invention is directed at providing programmable interrupt priorities within the context of pre-existing architecturally fixed priorities. Thus, off-core interrupts, which have architecturally fixed priorities, are not programmably altered, nor are they required to have pre-programmed interrupt priority levels. See Specification, paragraph [0040]. Thus, Applicant's "interrupt handler" prioritizes interrupts from two sources, one of which utilizes programmable interrupts, the second of which utilizes architecturally fixed priorities. Further, Applicant is not redesigning an external interrupt handler. Applicant is using an interrupt handler that already exists, which has architecturally fixed interrupts for external interrupts, and couples this to a priority encoder and vector generator which utilizes a status register coupled thereto to programmably define interrupt priorities for internally generated interrupts, which are the same as, are in between the interrupt priority levels fixed at the interrupt handler. Thus, applicant's invention can be implemented into pre-existing architectures, improving the performance of interrupts for on-chip interrupts, while still servicing external interrupts in a legacy fashion. Beckert, on the other hand, requires that ALL interrupts contain programmed priority levels for his device to function - something that would require significant redesign, and additional cost for his interrupt handler.

With the above background in mind, applicant will now respond to the examiner's rejections.

With respect to claim 1, it is repeated below, as amended, for ease of reference:

1. (currently amended) A processing system comprising:

a plurality of first interrupts generated by a core, said plurality of first interrupts having programmable priorities;

a plurality of second interrupts that are generated external to said core, said second interrupts having architecturally fixed interrupt priorities;

a status register, coupled to said core, said status register comprising a vector table, and an interrupt register, said interrupt register coupled to said vector table, said interrupt register having a plurality of configurable priority registers for storing said programmable priorities; and

a priority encoder, coupled to both said first interrupts and to said second interrupts, and to said status register, said priority encoder prioritizing said first and second pluralities of interrupts utilizing said programmable priorities for said first interrupts and said architecturally fixed interrupt priorities for said second interrupts.

The examiner indicated that among the items taught by Larsen, that Larsen does not teach that a plurality of first interrupts having programmable priorities; said programmable priorities being different than those architected for said plurality of second interrupts. So, the Examiner has utilized Beckert to show an interrupt handler having configurable priority registers for storing programmable priorities different than architected priorities. Applicant respectfully traverses.

As stated above, nowhere does Beckert show a priority encoder which prioritizes between a first and second pluralities of interrupts, the first interrupts having programmable priorities and the second interrupts having architecturally fixed interrupt priorities. Rather, Beckert requires that ALL interrupts have programmable priorities. As mentioned above, utilizing the invention taught by Beckert would add significant cost to applicant's solution because it would require wholesale replacement of the external interrupt handler. Applicant has instead provided an elegant solution of dealing with external interrupts having architecturally fixed interrupts with programmable internal interrupts to provide optimized interrupt handling. Nothing in Larsen, taken alone or in combination teaches the novel combination as recited in claim 1. Applicant has found no suggestion or hint in either Larsen or Beckert to suggest their combination, other than their general reference to the field of interrupt handling. For all of these reasons, applicant respectfully requests the examiner to withdraw his rejection of claim 1.

The examiner has provided a somewhat lengthy office action, enumerating each of the dependent claims, citing a combination of Larsen and Becket, combined with each other, and often in combination with an additional reference. In most of the enumerations, the examiner utilizes the language "It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen and Beckert with ..." for example. However, there is never any specific indication showing a teaching or suggestion in the references to combine them with the teachings of another. Applicant reminds the examiner that "[o]bviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching suggestion or incentive supporting the combination." See In re Geiger, 815 F.2d 686. And, "It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious...[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." see In re Fritch 972 F.2d 1260.

With respect to claims 2-8, these depend from claim 1 and add further limitations which are neither anticipated nor obviated by Larsen, taken alone or in combination with Beckert. For the reasons stated above with respect to claim 1, applicant respectfully requests the examiner to withdraw his rejection of these claims.

With respect to claims 10, and 27, applicant has amended these claims to particularly claim a first set of interrupts that have architecturally fixed interrupt priorities and a second set of interrupts that have programmable priorities. These claims further require prioritizing or sorting of both types of interrupts, using both types of priorities, to find the highest level pending interrupt. Nothing in Larsen combined with Beckert teach this novel combination. For this reason, and for those stated above with respect to claim 1, applicant respectfully requests that the examiner withdraw his rejection of these claims.

With respect to claims 11-26, these depend from claim 10 and add further limitations which are neither anticipated nor obviated by Larsen/Beckert taken together, or in combination with the additionally recited references. For all of the reasons stated above

with respect to claims 1, 10 and 27, applicant respectfully requests the examiner to withdraw his rejection of these claims.

With respect to claims 28-32, these depend from claim 27 and add further limitations which are neither anticipated nor obviated by Larsen/Beckert taken together, or in combination with the additionally recited references. For all of the reasons stated above with respect to claims 1, 10 and 27, applicant respectfully requests the examiner to withdraw his rejection of these claims.

CLAIM REJECTIONS - 35 USC §101

The examiner rejected claims 37, 38 and 39 under 35 USC §101, because the claimed invention is directed at non-statutory subject matter. The examiner initially stated that claims 37, 38, 39 are directed to an intangible signal because the computer data signal is not contained on a tangible medium. Applicant traversed this argument in Amendment A. In the present office action, the examiner indicates that the transmission medium encompasses both tangible and intangible transmission mediums. Applicant believes that many examples of a tangible transmission mediums exist (e.g., wired-ethernet, wireless Ethernet, Bluetooth, etc.). However, Applicant is not aware of any intangible transmission medium. Applicant respectfully requests the examiner to provide an example of an intangible transmission medium. In any event, applicant has amended claim 37 to specifically recite a computer readable transmission medium. Since a computer readable transmission medium is tangible, applicant respectfully requests the examiner to withdraw his rejection of these claims.

The examiner requested applicant to resubmit the supplemental declaration so that it may be entered into the official record of the case. Applicant is resubmitting "Exhibit F" hereto.

Applicant has made an earnest attempt to respond to each of the examiner's rejections, and believes that by this amendment, that the present case is in condition for allowance.

Applicant earnestly requests the examiner to telephone him at the direct dial number printed below if the examiner has any questions or suggestions concerning the application.

Respectfully submitted,

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Date: 6-28-05

"EXPRESS MAIL" mailing label number EO 005 169 445 US Date of Deposit 6-29-05. I hereby certify that this paper is being deposited with the U.S. Postal Service Express Mail Post Office to Addressee Service under 37 C.F.R. §1.10 on the date shown above and is addressed to the U.S. Commissioner of Patents and Trademarks, Alexandria, VA, 22313.

By: Alicia Mercuri

Exhibit F

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	G. Michael Uhler
Serial No.:	09/977089
Filed:	10/12/2001
Docket:	MIPS:0139.00US
For:	CONFIGURABLE PRIORITIZATION OF CORE GENERATED INTERRUPTS

SUPPLEMENTAL DECLARATION

Assistant Commissioner for Patents
Washington, D.C. 20231

As a below named inventor, I hereby declare that:

In the originally submitted Declaration, the docket number and title indicated in the header were incorrect. They have been corrected in the header of this supplemental declaration.

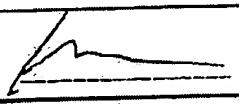
My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter claimed and for which a patent is sought on the invention referenced above, the specification of which ___ is attached hereto _X_ was filed on 10/12/2001 as U.S. Patent Application No. 09/977089.

I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to in this declaration.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Inventor's Name:	Residence and Post Office Address:	Citizenship:	Signature	Date
G. Michael Uhler	1852 Valparaiso Ave Menlo Park, CA 94025	US		6/14/02